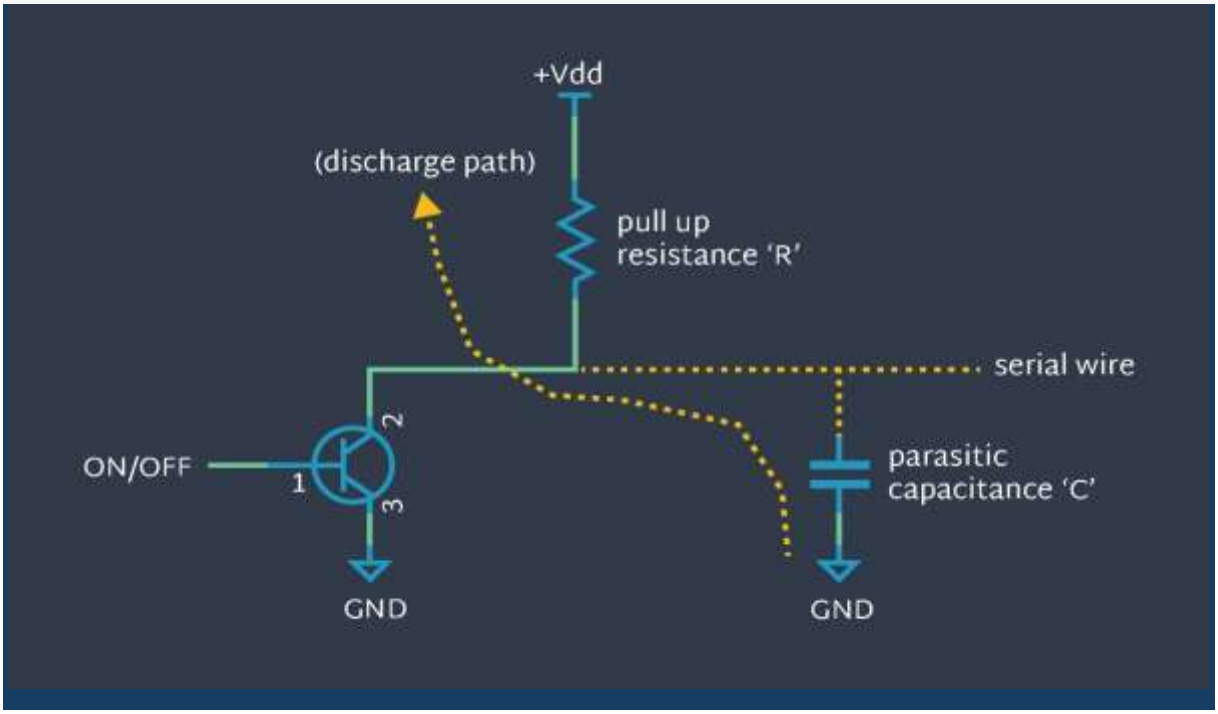

I²C Voltage Level Translators

I2C (Inter-Integrated Circuit) is a multi-master to multi-slave two-wire serial bus standard that enables serial […]

I²C (Inter-Integrated Circuit) is a multi-master to multi-slave two-wire serial bus standard that enables serial communications at a number of bit rates (depending upon supported mode) over several meters of cable. I²C is a relatively old, but still extremely popular standard that arrived on the scene in 1982.

Since then, 5V logic interfaces have given way to much lower voltage standards and I²C bus systems need to accommodate for level shifting to enable intercommunications with different interface voltage devices on the same bus. Communication data rates have also increased from the original 100 kHz clock rate to up to 5MHz in ultra-fast modes, and level shifting must be able to accommodate for these higher data rates.

I²C signaling comprises a single data signal that carries logic levels validated by a clock signal. Both signals are bidirectional, driven by one or more masters or slaves depending on the state of the system. In order to prevent damaging contention caused by outputs driving each other, open drain or open collector outputs with pull up resistors drive the bus.

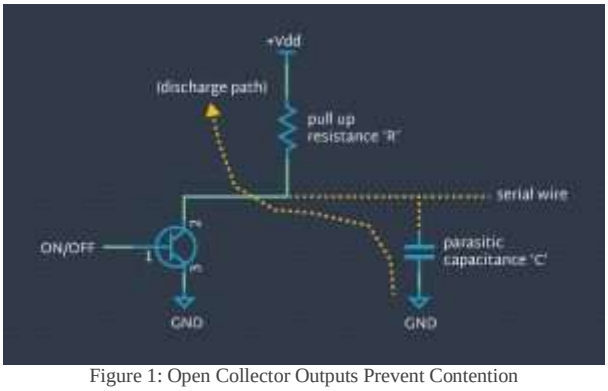

Figure 1: Open Collector Outputs Prevent Contention

An open drain (FET based) or open collector (BJT based) output is one that does not have an active gate pulling up to the positive supply. Turning the output gate off places the output in a high impedance state. The signal wire floats high as the charge stored by the bus capacitance discharges through the pull up resistance as shown in figure 1.

The speed of a transition between low to high on the signal bus is therefore limited by the time it takes for the electric charge stored on the parasitic capacitance on the wire 'C' to discharge through the pull-up resistance 'R', the 3dB point being defined by equation: $f_{3dB} = 1/(2\pi.R.C)$

For example, if the combined capacitive bus loading is 100pF, and combined pull-up resistance on the signals on the bus being 1.5kΩ, the 3dB point is approximately 1MHz. This limits the maximum data rate possible on the bus but has the clear benefit of never having a situation where low impedance outputs drive each other, causing damaging high currents to flow through the gate. The bidirectional nature of I^2C signals, the variation of bus voltage levels and the open drain output requirements considerably complicate level translation circuitry.

Logic Levels Compatibility

Different logic levels have different logic threshold voltages that determine the high/low logic transition. Different voltage standards also cause issues due to the presence of diode junctions on input and outputs of semiconductor devices. Signal levels driven higher than the supply voltage force the diode into conduction in a destructive condition called "latch-up".

I^2C has traditionally complied with 5V logic standards, but potentially needs to work with many other lower voltage interface standards. Even when the interface standard thresholds and regions seem within acceptable ranges, reduced noise margins compromise bus performance without proper logic level translation.

Figure 2: Typical Logic Family Voltage Levels

A bus system must be compatible with the worst-case combination of logic levels relating to the individual devices over the device variation and anticipated temperature range. Make note that each device on the common bus increases capacitance and may further reduce margins. Single-ended buses, especially ones with long wires, are subject to impedances on the ground or supply that cause edge ringing and ground bounce – effects that further reduce level margins.

The use of a bidirectional buffer may not specifically offer different voltage translation, but it can help maintain voltage tolerances where the signal levels are compatible between standards. I²C Repeaters also provide a way to isolate the capacitive load of a bus by splitting it into two, extending cable runs or number of devices supportable in a system. I²C interfaces are very tolerant of long cable runs due to the low data rate, 5V signalling support and the open drain nature. These characteristics lead it to use in situations where devices plugged in and out of the serial bus add complexity of level translation circuitry and exposed connections add the requirement for electrostatic discharge (ESD) protection.

Discrete MOSFET Method of Level Translation

Bidirectional level shifting must conduct in both directions. The simplest method uses MOSFETs as depicted in figure 3, and described in more detail in application note AN10441. Although a MOSFET level shifter is acceptable for 100kHz to 400kHz communications standards, it does not have the performance required for faster modes of operation due to the previously mentioned frequency limitations imposed by RC time constants. In cases where higher bandwidth modes are used, special purpose level translator devices are required.

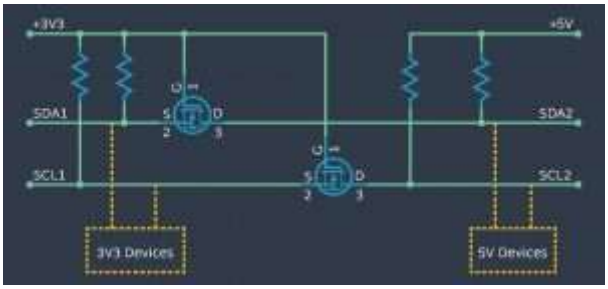

Figure 3: MOSFET Based Level Translation

I²C interfaces have positive going edges limited by this effect. The MOSFET circuit introduces additional parasitic capacitances (for example the Miller effect) and switching levels that further distort the characteristics of both edges during direction changes. This can

cause problems if the logic interface is marginal as they have a transition region around the threshold voltage where the output is indeterminate.

Signals that reside inside this range cause what is termed ‘meta-stable states’ that cause signal glitching. Schmitt trigger inputs are special interfaces with voltage hysteresis caused by positive feedback from the input gate output. This increases noise margin and reduces the potential for metastability due to slowly changing signals.

Also, noisy, slow or non-monotonic signals, can exist on I²C serial buses are also corrected using a debounce algorithm. A debounce algorithm introduces a dwell time where the input signal is monitored over a time period for a continuous signal level before changing, rejecting glitch transitions that fall within this period. This is a technique used with FPGAs and ‘bit-banging’ software implementations on microcontrollers.

Isolated Methods

A system as described in figure 4 is a non-isolated system with direct electrical connection between the two devices, irrespective of the voltage level translation. As I²C interfaces are unbalanced and can have long cable interconnects, these potential differences can lead to spurious noise currents on ground signals. Non-isolated grounds can lead to dangerous fault conditions when dealing with high voltage circuits. I²C interfaces used in applications that cross isolation boundaries have to meet safety standards and require galvanic isolation.

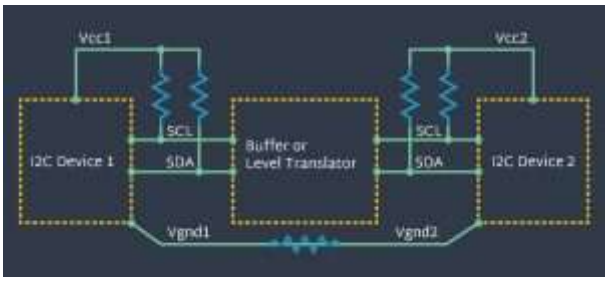

Figure 4: Non-Isolated Level Translation

The common method of electrically isolating I²C buses also incorporates level translation as the isolation boundary and enables any voltage support on either side of the isolation boundary. Conventional isolation techniques include photovoltaic isolation via opto-couplers or devices that modulate serial bus signal information across a capacitive bridge or inductive transformer.

All these tend to share the common characteristic of splitting/recombining the bidirectional signals into two unidirectional paths. Some applications extend the length of cable supported and increase noise immunity by converting the signals to a differential standard (like RS485). They may also utilize higher signalling voltages.

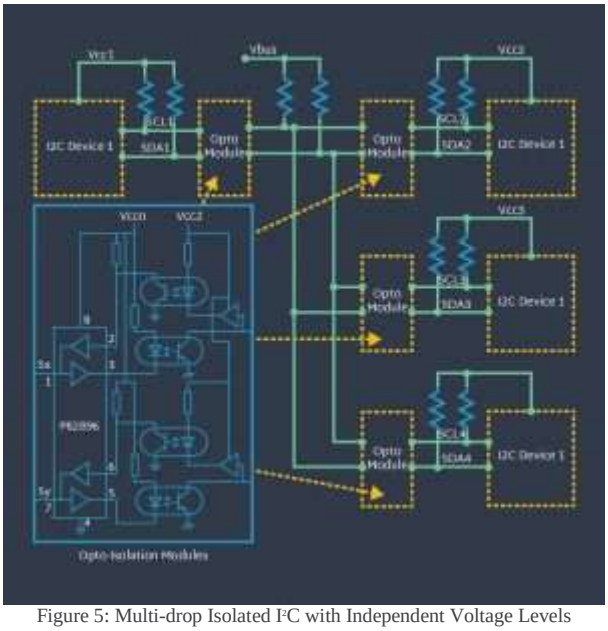

Figure 5: Multi-drop Isolated I²C with Independent Voltage Levels

Opto-electrical isolation of the I²C-bus, like the circuit described in figure 5, is capable of operating at speeds in excess of 1Mbps. NXP's application note AN10364 is a comprehensive description of various topologies for interfacing between I²C devices with different local ground potentials and voltages. Similar topologies are found in applications that require primary to secondary side communications in isolated AC mains power circuits, medical equipment and Power of Ethernet (PoE).

Bidirectional Voltage Level Translators

Bidirectional voltage translators can work on an I²C bus. It is important to ensure the device is the correct bus orientation – matching the bus voltage level to the correct translator side. Most translators will specify one side to be greater than a minimum voltage (typically around 1V) than the other side. Both sides will still require pull-ups for correct I²C operation as described in application note AN11127.

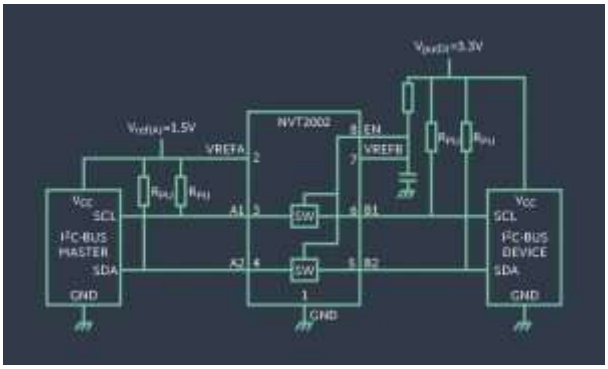

Figure 6: Bidirectional Level Translator in I²C Circuit

Such devices are excellent for supporting I²C connection from 5V and 3V3 slave peripherals to low voltage I/O banks of FPGAs or microcontrollers. Dual open drain bidirectional voltage level translator devices such as the NVT2001 simplify multi-voltage bus architectures due to the low component count, high flexibility of solution, integrated ESD protection and the tiny physical packages.

They also serve to provide isolation between slower and faster elements on an I^2C bus, enabling them to interoperate in the same design. Controlling the enable pin to disconnect slower buses during fast mode communications provides for coexistence. These devices feature less than 1.5ns propagation delay (not including bus loading) and 33MHz clock performance in an open drain system. High frequency support enable solutions for ultra-fast modes of operation to incorporate level shifting and raises the possibility of even higher speed I^2C interface standards in future.